549,561

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 September 2004 (30.09.2004)

PCT

(10) International Publication Number
WO 2004/084404 A1

(51) International Patent Classification[7]: H03F 1/30, H03H 11/24

(21) International Application Number: PCT/IB2004/000752

(22) International Filing Date: 16 March 2004 (16.03.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
03100720.6 20 March 2003 (20.03.2003) EP

(71) Applicant *(for DE only)*: **PHILIPS INTELLECTUAL PROPERTY & STANDARDS GMBH** [DE/DE]; Steindamm 94, 20099 Hamburg (DE).

(71) Applicant *(for all designated States except DE, US)*: **KONINKLIJKE PHILIPS ELECTRONICS N. V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **BRILKA, Joachim** [DE/DE]; c/o Philips Intellectual Property & Standards GmbH, Weisshausstr. 2, 52066 Aachen (DE). **KATTNER, Axel** [DE/DE]; c/o Philips Intellectual Property & Standards GmbH, Weisshausstr. 2, 52066 Aachen (DE). **RAGOSCH, Ernst-Peter** [DE/DE]; c/o Philips Intellectual Property & Standards GmbH, Weisshausstr. 2, 52066 Aachen (DE).

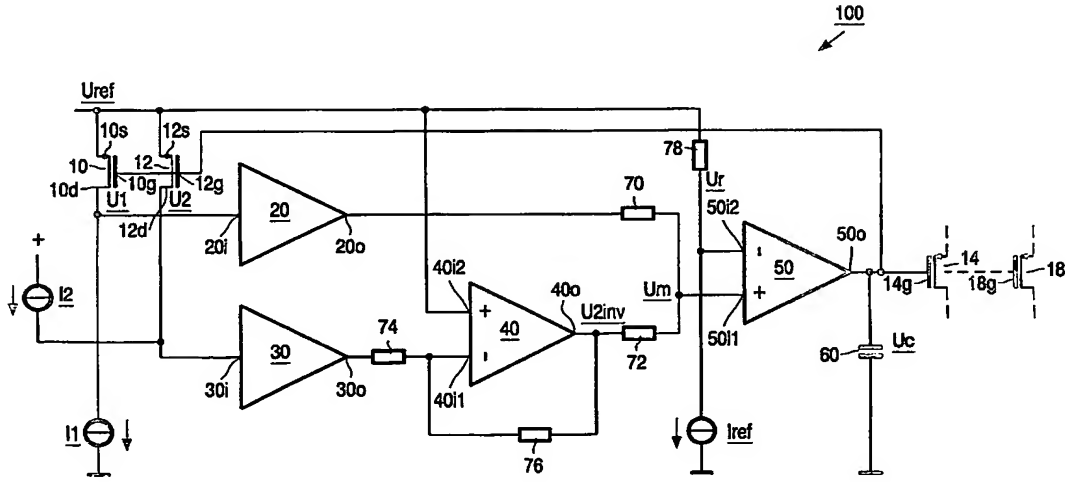
(74) Agent: **VOLMER, Georg**; Philips Intellectual Property & Standards GmbH, Weisshausstr. 2, 52066 Aachen (DE).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),

[Continued on next page]

(54) Title: CIRCUIT ARRANGEMENT AND TRANSISTOR CONTROL METHOD



(57) Abstract: In order to improve a circuit arrangement (100) and a method of controlling at least one transistor (10, 12, 14, , 18), especially of controlling the resistance value of at least one MOS transistor with vanishing DC modulation in such a way that a compensation of resistance variations without control deviation is also possible for the case where the transistor (10 , 12 , 14, , 18) is operated with a vanishing DC voltage, i.e. with a zero DC voltage and indeed without the aid of a reference frequency, it is suggested that in addition to at least a first reference element (10, 20, 70), which has at least a first reference transistor (10) with a first offset from the operating point, at least a second reference element (12, 30, 40, 72 ,74, 76) is provided which has at least a second reference transistor (12) with a second offset from the operating point equal in value but opposed in sign to the first buffer storage, wherein an in particular arithmetic average can be formed from the first offset and the second offset for approximating and achieving an optimum operating point.

WO 2004/084404 A1

Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.